

WHAT IS CLAIMED IS:

1. A diode, comprising:

2 a substrate doped with a first type dopant; and

3 a double implanted guard ring located within said substrate
4 and doped with a second type dopant opposite said first type dopant
5 and having a first doped profile region and a second doped profile
6 region.

2. The diode as recited in Claim 1 further including an
2 electrode located over said substrate and an isolation region
3 located adjacent said electrode, wherein said first doped profile
4 region extends more than about 1 μm under said isolation region.

3. The diode as recited in Claim 2 wherein said guard ring
2 has a profile that provides an impact ionization rate of about $3\text{E}17$
3 $\text{cm}^{-3}/\text{second}$ at an interface of said guard ring and said isolation
4 region during operation of said diode.

4. The diode as recited in Claim 2 wherein said diode has a
2 reversed breakdown voltage ranging from about 28 volts to about 36
3 volts or greater and with a leakage current of less than about $1\text{e}-$
4 10 amperes.

5. The diode as recited in Claim 1 wherein first doped

2 profile region has a doping concentration less than said second
3 doped profile region.

6. The diode as recited in Claim 5 wherein said first doped
2 profile region has a p-type doping concentration of about 6×10^{15}
3 atoms/cm³ and said second doped profile region has a p-type doping
4 concentration of about 5×10^{19} atoms/cm³.

7. The diode as recited in Claim 1 wherein said second doped
2 region is located at least partially within said first doped
3 profile region.

8. The diode as recited in Claim 1 further including an
2 electrode located over said substrate and an isolation region
3 located adjacent said electrode and wherein said first doped
4 profile region has a profile that substantially covers an electric
5 field extending through said isolation region and said substrate
6 during operation of said diode.

9. A method of fabricating a diode in an integrated circuit,
2 comprising:

3 doping a substrate with a first type dopant; and
4 forming a double implanted guard ring within said substrate by
5 doping with a second type dopant opposite said first type dopant to
6 form a first doped profile region and a second doped profile
7 region.

10. The method as recited in Claim 9 further including
2 forming an electrode over said substrate and forming an isolation
3 region adjacent said electrode such that said first doped profile
4 region extends more than about 1 μm under said isolation region.

11. The method as recited in Claim 10 wherein forming said
2 guard ring includes forming said guard ring to have a profile that
3 provides an impact ionization rate of about $3\text{E}17 \text{ cm}^{-3}/\text{second}$ at an
4 interface of said guard ring and said isolation region during
5 operation of said diode.

12. The method as recited in Claim 10 wherein said diode has
2 a reversed breakdown voltage ranging from about 28 volts to about
3 36 volts or greater and with a leakage current of less than $1\text{e-}10$
4 amperes.

13. The method as recited in Claim 9 further including
2 forming well regions and source/drain regions for a plurality of
3 transistors and wherein said first doped profile region is a well
4 region formed simultaneously with said well regions of said
5 plurality of transistors and said second doped profile is a
6 source/drain region formed simultaneously with said source/drain
7 regions of transistors.

14. The method as recited in Claim 9 wherein said first doped
2 profile region has a doping concentration less than a doping
3 concentration of said second doped profile region.

15. The method as recited in Claim 9 further including
2 forming an electrode over said substrate and forming an isolation
3 region adjacent said electrode such that said first doped profile
4 region has a profile that substantially covers an electric field
5 extending through said isolation region and said substrate during
6 operation of said diode.

16. The method as recited in Claim 9 wherein said second
doped region is located at least partially within said first doped
profile region.

17. An integrated circuit, comprising:

CMOS transistors;

bipolar transistors;

diodes, wherein each diode includes:

a substrate doped with a first type dopant;

an electrode located over said substrate;

an isolation region located adjacent said electrode; and

a guard ring located within said substrate and doped with

a second type dopant opposite said first type dopant and having a

first doped profile region and a second doped profile region,

wherein said second doped region is located at least partially

within said first doped profile region; and

interconnects that interconnect said CMOS transistors, bipolar transistors and diodes to form an operative integrated circuit.

18. The integrated circuit as recited in Claim 17 wherein said first doped profile region extends more than about 1 μm under said isolation region such that said first doped profile region has a profile that substantially covers an electric field extending through said isolation region and said substrate during operation of said diode.

19. The integrated circuit as recited in Claim 18 wherein said guard ring has a profile that provides an impact ionization

3 rate of about $3E17 \text{ cm}^{-3}$ /second at an interface of said guard ring
4 and said isolation region during operation of said diode.

20. The integrated circuit as recited in Claim 17 wherein
2 said CMOS transistors includes p-typed doped wells and p-type doped
3 source/drains and each of said first doped profile regions is a
4 well region having a doping concentration similar to said p-type
5 doped wells and each of said second doped profiles is a
6 source/drain region having a doping concentration similar to said
7 p-type doped source/drains regions.

21. The integrated circuit as recited in Claim 17 wherein
2 said first doped profile region has a doping concentration less
3 than a doping concentration of said second doped profile region.